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THD Effectiveness of Five-Level Inverters: CHB vs. NPC

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***Abstract*—In this study, two popular multilevel inverter topologies—the Neutral Point Clamped (NPC) and the Cascaded H-Bridge (CHB)—are compared. Identical variables are used to assess the two distinct kinds of inverters: 50Hz as the working frequency and 380V RMS for the voltage from the line. To ascertain the expected results of every kind of inverter, simulating analyses were carried out on THD, switching loss, and waveform integrity. The study's findings show that although both kinds of multilevel inverters are capable of producing multilevel voltage through synthesis, the CHB outperforms the NPC inverter with regard to of THD and harmonic distortion and may produce multilevel voltage to a wider variety of techniques for modulation (phase-to-phase shifting). Additionally, the NPC uses smaller components and has a simpler DC end connecting architecture, which may be advantageous in certain situations where expense and reliability are crucial. These findings can therefore help in the selection of an inverter topology to satisfy the demands of powerful (over 1MGA), medium voltage (3–15kV) scenarios that demand superior efficiency, THD, and intricate topological development concerns. For 5-level, three-phase structures, CHB is more effective at producing THD and harmonic efficiency than NPC, even though NPC has a simpler design and a much lower practical footprint.**

Keywords—Whole distortion of harmonics, three-phase, five-level CHB and NPC inverters, and MATLAB/Simulink predictive models

I. INTRODUCTION

In modern electric facilities multilayer inverters, or MLIs, are becoming more and more well-known for achieving increased power reliability with minimal harmonic distortion. By producing stepping voltage waveforms that closely match sinusoidal outcomes, MLIs reduce transferring stress and improve electromagnetic overall performance when compared to traditional -stage inverters. Despite their respective drawbacks, impartial factor Clamped (NPC) and Cascaded H-Bridge (CHB) are two of the most often used topologies. This work provides a single evaluation method that examines structures under the same situations, with a focus on the general effectiveness of Harmonic Distortion (THD) [1], [2], [3], [4], [5], [6]. NPC inverters are a good way to exploit distant DC assets, but they need more clamping diodes and have more complicated voltage balance issues. [7], [8]. The harmonic readability of the inverter output is the most important feature to examine for MLIs. Unwanted consequences include electromagnetic field interference, increased copper and internal losses, and decreased device and strength element effectiveness due to harmonics. [4], [9].

General harmonic distortion, or THD, is a quantifiable measure of a waveform's departure from a sinusoidal structure. THD for voltage is most likely expressed as:

$$THD_v = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V1}\ X\ 100\%$$

Where:

- V stands for basic element The amplitude of RMS
- The RMS amplitude of the nth harmonic component is denoted by Vn..
- N ≥ 2.

A reduced THD indicates a wave pattern that closely resembles a perfect sinusoidal pattern. International standards such as IEEE Std state that in most power topologies, the voltage THD at the points of common coupling (PCC) should not exceed 5%. 519-2014 [10]. In contrast, the CHB inverter generates greater voltage levels by connecting several isolated DC sources in series using cascaded H-bridge cells.[11]. This modular architecture provides outstanding scalability, redundancy, and fault tolerance for renewable energy systems, such as solar and battery-based energy storage applications. [2], [3]. Furthermore, for CHB inverters, phase-shifted or level-shifted PWM approaches simplify voltage stabilization and enhance harmonic performance. [12].

among the most crucial performance metrics for evaluating inverter architectures is total harmonic distortion, or THD. High harmonic activity can lead to delicate machinery faults, increased copper and core losses, electrical machine heating up, and grid-code problems. [9], [13]. International standards such as IEEE Std. 519-2014 state that voltage THD at the point of common coupling (PCC) should not be greater than 5% for the majority of power systems. [4]. Several investigations have already been conducted on harmonic mitigation strategies for multilevel inverters, including advanced PWM programs, particular harmonic elimination (SHE), and enhanced carrier-based modulation. [5], [14]. Direct performance comparisons are made more difficult by the fact that many published studies either focus on a single topology or use

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different operating circumstances, modulation indices, or switching frequencies. [15], [16]. Additionally, there are still a few systematic studies that particularly target five-level NPC and CHB inverters under consistent conditions, even though higher-level inverters (seven-level and above) have been thoroughly examined.

A. Novelty and Contribution Statement:

A consistent quantitative comparison between three-level CHB and NPC inverters under the same operating and modulation settings is still scarce in the literature, despite the growth of multilevel converter research. There is a realistic comparative analysis gaps for mid-level procedures where effectiveness, ease of use, and harmonic purity have to be optimized simultaneously due to previous research typically only considers architecture or takes higher-level designs (five-level and above) into consideration. The present research bridges the gap by developing detailed MATLAB/Simulink models of three-phase, three-level CHB and NPC inverters operating with the same physical boundary circumstances (380 V RMS line voltage, 50 Hz, SPWM modulation, and 2 kHz switching frequency). The benefit of this article might be summarized up as follows:

1. Universal comparison modeling: the two architectures have been replicated using identical methods of modulation and parameters with the same values.
2. Precise harmonic evaluation: THD evaluation with FFT and final voltage spectrum profile.
3. Productivity comparing notes: evaluating the effects of its modularity, control difficulty, and switching losses.
4. Designing suggestions: suggestions for medium-voltage drive and renewable energy resource connection architecture selection.

The research presented here stands out from others thanks to its repeatable simulation, thorough evaluation of performance, and uniform simulation conditions. It also offers an obvious resource for design and engineering improvement.

II. METHODOLOGY

The Total Harmonic Distortion (THD) performance of five-level, three-phase inverters with Neutral Point Clamped (NPC) and Cascaded H-Bridge (CHB) topologies is assessed in this study. MATLAB/Simulink is used to model and simulate both inverters under identical operating conditions in order to provide a fair and consistent comparison. The same electrical characteristics were used to mimic both inverter topologies. The system runs at a fundamental frequency of 50 Hz with a rated line-to-line voltage of 380 V RMS as listed in Table I. A three-phase RL load that was balanced was used.

TABLE I. SUMMARISES IMPORTANT SIMULATION PARAMETERS.

Parameter	Value
Line-to-line RMS voltage, V_LL	380 V
Frequency	50 Hz
Phase RMS voltage, V_ph	219.4 V
Carrier frequency	5 kHz
Modulation	SPWM
Load	Balanced three-phase RL

Using a carrier frequency of 5 kHz, sinusoidal pulse width modulation (SPWM) was employed. To guarantee steady-state harmonic analysis, the simulation's duration was set at 0.1 seconds.

A. The 5-Level NPC Topology (Diode-Clamped Multilevel Inverter):

NPC signifies an evolution of the conventional diode-clamped (or neutral-point clamped) inverter design. It utilises DC-link capacitors, power switches (IGBTs/MOSFETs), and clamping diodes to generate multiple voltage levels at the output. DC-Link Capacitors: The DC bus is divided into (N–1) capacitors for an N-level inverter. For a 5-level inverter, 4 capacitors split the total DC bus voltage Vdc into four equal parts (Vdc/4). Switches: Each phase leg consists of (N–1) × 2 = 8 switches. Clamping Diodes: Additional diodes connect switch nodes to the neutral points of the DC bus, thus clamping the voltage across the switches. Output Levels: The inverter can produce +Vdc/2, +Vdc/4, 0, -Vdc/4, -Vdc/2. Phase-Leg Operation (5-Level NPC). A single leg can produce five voltage states concerning the DC neutral point: +Vdc/2 → top switches ON. +Vdc/4 → a combination of top and middle switches with clamping diodes. 0 → middle switches conducting. -Vdc/4 → a combination of bottom and middle switches with diodes. -Vdc/2 → bottom switches ON as depicted in Figure 1.

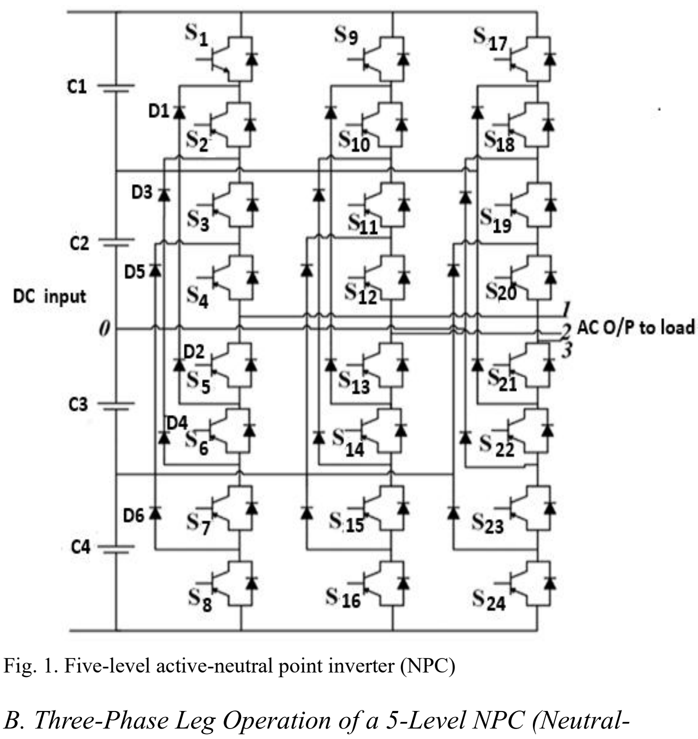

Fig. 1. Five-level active-neutral point inverter (NPC)

B. Three-Phase Leg Operation of a 5-Level NPC (Neutral-Point-Clamped).

Figure 2 shows the single-phase leg of a 5-level NPC inverter, which consists of 8 IGBTs/MOSFETs (S1–S8), 6 clamping diodes (D1–D6), and 4 DC-link capacitors (C1–C4), which divide the DC bus into 5 distinct voltage levels: +2Vdc, +Vdc, 0, –Vdc, and –2Vdc. The capacitors (C1–C4) create the split DC bus, with each capacitor maintaining an equal voltage of (Vdc/2), thus forming the neutral point and intermediate nodes. The switches (S1–S8) control the current path and the output level. The clamping diodes (D1–D6) connect the intermediate switch nodes to the neutral capacitor nodes, ensuring voltage balance and safe commutation. The output terminal is capable of delivering five levels: +2Vdc, +Vdc, 0, –Vdc, and –2Vdc. This demonstrates which switches (S1–S8) are engaged to achieve each output level at the phase terminal.

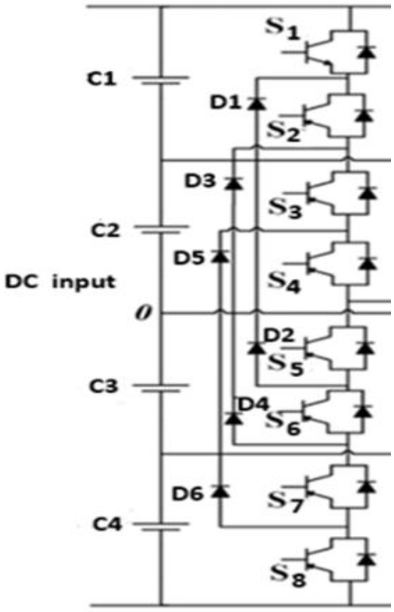

Fig. 2. Phase Leg Operation of a 5-Level NPC (Neutral-Point-Clamped) Inverter in detail.

TABLE II. 5-LEVEL, 3-PHASE SWITCHING TABLE FOR NPC SINGLE LEG

Output Voltage on leg one	S1	S2	S3	S4	S5	S6	S7	S8
+Vdc	1	0	1	0	1	0	1	0
+Vdc/2	1	0	1	0	1	0	0	1
0	1	0	0	1	1	0	0	1
-Vdc/2	0	1	0	1	0	1	0	1
-Vdc	0	1	0	1	0	1	0	1

• "1" indicates the switch is ON, while "0" signifies the switch is OFF.
• Table II illustrates the phase leg switching necessary to produce the intended 5-level output.
Numerical DC-link sizing for a 380 V (line-to-line), 50 Hz system. It likely wants the 3-phase line RMS = 380 V (L-L). For a star-connected inverter, the phase (line-to-neutral) rms is:
Step-by-step calculation (digit by digit) as follows:

- $V_{LL,\ rms}$ = 380.000 V
- $V_{LN\ rms}$= $V_{LL\ rms}$ / $\sqrt{3}$ = 380/1.732= 219.4 V.
- Phase peak = $V_{LN,\ peak}$ = 219.4 X $\sqrt{2}$ = 310.27 V.
- Phase peak: For 5-level symmetric levels (−2Vs, −Vs,0, +Vs, +2Vs), so:
- Vs = $V_{LN,\ peak}$ / 2 = 310.27 / 2 = 155.134
- Total DC bus = (4 x 155.134) = 620. 54 V

A three-phase, five-level Cascaded H-Bridge (CHB) inverter. Let us analyse it thoroughly and draw a text-based schematic. Key Details for a 5-Level CHB Inverter:

- Levels per phase: 5
- Number of H-bridges per phase:2 H-bridges per phase
- Switches per H-bridge: 4 → 8 switches per phase
- Three phases: A, B, C
- Voltage sources: DC1, DC2 per phase

C. A three-phase, five-level Cascaded H-Bridge (CHB) inverter.

According to Figure 3, it shows, the key Details for a 5-Level CHB Inverter:

- Number of H-bridges per phase: 2 H-bridges per phase
- Switches per H-bridge: 4 → 8 switches per phase
- Three phases: A, B, C
- Voltage sources: DC1, DC2 per phase.

Notes:

D. Voltage Levels per Phase

Output voltage levels = −Vdc2, −Vdc2, 0, +Vdc2, + Vdc1+Vdc2.With 2 H-bridges in series per phase, you can generate 5 voltage levels.

E. Series Connection

The two H-bridges per phase are cascaded in series as shown in Figure 4. The three phases are independently cascaded for a three-phase load.

F. Switching Strategy

Each H-bridge is switched independently to create the multilevel waveform. For a 5-level output, there are specific switching states for each H-bridge to achieve the ±Vdc1, ±Vdc2, and 0 levels.

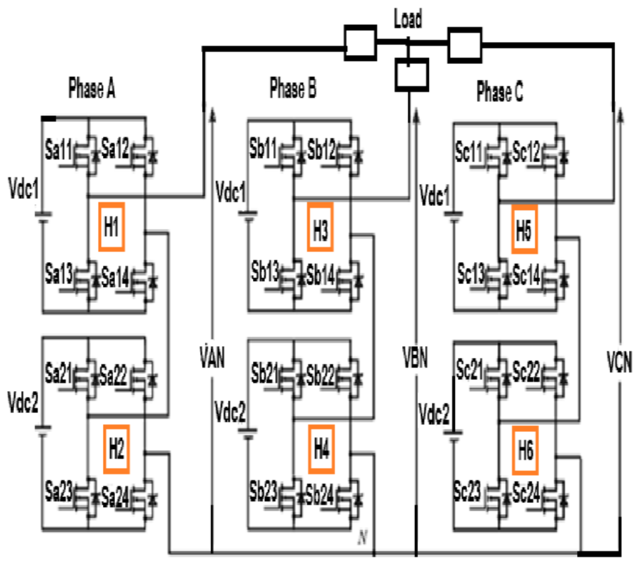

Fig. 3. Five-level, three-phase Cascaded H-Bridge (CHB) inverter

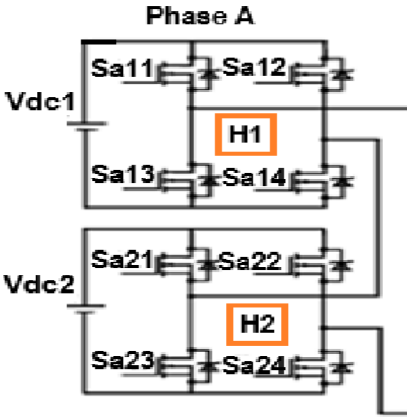

Fig. 4. Two H-bridges in series per phase for a 3-phase, 5-level CHB inverter

In the context of carrier-based PWM, each cell should be modulated independently using suitable phase-shift and level-shift carriers to create a stepped waveform characterised by low harmonic distortion. Each phase leg (A, B, C) consists of two H-bridge cells arranged in series. Each H-bridge cell operates with its own isolated DC source (Vdc/2). By merging the outputs of two cascaded cells, each phase is capable of generating five levels: {+Vdc, +Vdc/2, 0, −Vdc/2, −Vdc}.
For every H-bridge cell, the standard states are defined as follows: +1 corresponds to an output of +Vdc, 0 indicates an output of 0 (achieved through leg shorting), and -1 signifies an output of -Vdc. Each H-bridge will be denoted by the states +, 0, and -.

TABLE III. A TABLE ILLUSTRATING THE SWITCHING STATES FOR TWO H-BRIDGES PER PHASE.

Cell Upper	Cell bottom	Resulting Level (sum)	Numeric level
-	-	-2 Vdc	-2
-	0	-1 Vdc	-1
0	0	0	0
+	0	+1 Vdc	+1
+	+	+2 Vdc	+2

DC Link Sizing per H-Bridge Cell for a 5-level CHB inverter, as shown in Table III:

- Levels: -2, -1, 0, +1, +2
- RMS line voltage $V_{LL, RMS}$=380
- Phase voltage $V_{ph\ rms}=V_{LL\ rms}/\sqrt{3}\approx 219.4$ V

Assuming each H-bridge cell is supplied by equal DC sources:

- 2 H-bridge cells per phase → output levels: −2Vdc, −Vdc, 0, +Vdc, +2Vdc, maximum phase voltage (peak) = $V_{ph\ peak} = V_{ph\ RMS} \times \sqrt{2} \approx 310\ V_{ph\ peak}$

G. Set DC per cell:

Vdc = $V_{ph,\ peak}$ / 2 ≈ 310 /2 =155 V. Therefore, each H-bridge cell should have Vdc ≈ 155 V. Therefore, switching produces: -2Vdc, -Vdc, 0, +Vdc, +2Vdc → - 310 V, -155 V, 0, +155 V, +310 V.

TABLE IV. SWITCHING TABLE FOR TWO H-BRIDGES PER PHASES A, B, AND C

Cell Upper	Cell Bottom	Phase Output (V)	Numeric Level
-	-	-310	-2
-	0	-155	-1
0	0	0	0
+	0	155	1
+	+	310	2

The Three Phase Block View (380 V system), it is as follows, illustrating each H cell for the three phases as presented in Table IV:
Phase A: H1 + H2 (DC 155V each) → V_a
Phase B: H3 + H4 (DC 155V each) → V_b
Phase C: H5 + H6 (DC 155V each) → V_c
For a 3-phase load, connected in either Y or Δ configuration, the details are as follows and are presented in Table IV:

- Each H-bridge operates at 155 V DC
- Maximum line-to-neutral voltage: 310 V
- Line-to-line voltage: 380 V RMS

H. Timing / Stepped Waveform

- Frequency: 50 Hz (fundamental).
- Each H-bridge can utilize phase-shifted PWM.
- Output voltage steps: -310, -155, 0, +155, +310 V (peak) as shown in Table IV.

- Step width: Ts = 1/50 = 20 ms, Ts =1/50 = 20 ms per fundamental cycle.

I. The Modulation Technique and THD Calculation

For both inverter topologies, sinusoidal PWM (SPWM) was used to guarantee constant modulation conditions. Fast Fourier Transform (FFT) analysis was used to determine the output voltage's harmonic content. The Total Harmonic Distortion (THD) of voltage is calculated as follows:

$$THD_v = \frac{\sqrt{\sum_{n=2}^{N} V_n^2}}{V_1} \times 100\%$$

Where V_n is the RMS value of the nth harmonic component, and V_1 is the RMS value of the fundamental component.

III. DISCUSSION AND RESULTS

These inverters produce an output voltage with five distinct voltage levels and are a specialised type of multilayer inverter (MLI). These levels are usually obtained by dividing a single DC source using capacitors or other methods, or by combining multiple DC voltage sources. Unlike a typical 2-level inverter, which merely alternates between +V and -V, the outcome is a stepped AC waveform that nearly resembles a sine wave. This section displays and discusses the simulation results from the three-phase, five-level NPC and CHB inverters operating under the same electrical and modulation parameters. Evaluation focuses on ultimate voltage structures, harmonic spectrum, and total harmonic distortion (THD) accomplishment.

A. Evaluation of THD and Harmonic Spectrum

The ensuing voltage harmonics spectra for both layouts is displayed in Figure 5. A steady-state FFT analysis was performed to guarantee precise harmonic representations. The NPC inverter is dominated by lower-order harmonics, particularly the fifth and seventh elements. Such harmonics are common in diode-clamped devices and are impacted by neutral-point voltage fluctuations and switching constraints. In contrast, the CHB inverter exhibits a notable decrease in easier harmonics, since the major harmonics shift to higher orders (11th and 13th) and display lesser scales. This harmonic spread phenomenon is caused by the phase-shifting PWM technique and cascaded design, which effectively distribute harmonic energy throughout greater frequencies. The CHB inverter generates a lower THD of approximately 2.9%, which is considerably within the suggested limits specified by IEEE Std. 519-2014, whereas the NPC inverter displays a THD of approximately 4.8%.

B. Comparative assessment of the performance of NPC and CHB

An overview of the THD performance contrast among the two inverter architectures is shown in Table V. Because of its higher voltage level synthesizing and modular structure, the CHB inverter outperforms the NPC inverter in regards to harmonic purity. However, this improved harmonic effectiveness leads to more intricate electronics and the need for more separate DC supplies. Although having a higher THD, the NPC inverter offers benefits such a simplified DC-link construction, fewer components, and a lower system budget. Thus, the particular needs of the application determine which of the NPC and CHB architectures to use. The CHB design is more expected to be advantageous for systems that prioritize improved reliability and flexibility, such as those that integrate renewable energy sources with energy storage. On the other hand, applications like industrial motor drives that value affordability, simplicity, and compactness can favour the NPC topology.

C. The Voltage Source wave patterns

The phase and line voltage waveforms of the five-level NPC and CHB inverters running at 50 Hz and 380 V (line-to-line) are shown in Figure 6. Proper multilevel functioning is confirmed by the successful generation of stepping voltage waves with sinusoidal forms by both architectures. Although there are slight waveform distortions at zero-crossings, the NPC inverter produces a symmetrical five-level waveform. The employment of clamping diodes and neutral-point voltage imbalances are the primary causes of these distortions. On the other hand, the CHB inverter has an voltage stepping pattern and smoother level transitions. Improved voltage generation is made possible by the separate control of each H-bridge cell, producing waveforms that precisely match an ideal sinusoid.Table V evaluates the performance and the technical comparison of each topology. Figure 5 illustrates the total harmonics generated by the two topologies, CHB and NPC inverters, specifically the 5-level NPC and CHB inverters operating at 380 V RMS and 50 Hz. The system employed has the following configuration (identical for both):

- Voltage: 380 V RMS (line-line), approximately 540 V peak
- Frequency: 50 Hz
- Load: Balanced 3-phase RL load
- Carrier Frequency: 2 kHz – 5 kHz
- Modulation Technique: Sinusoidal PWM (SPWM)
- Simulation Time: 0.1 s

TABLE V. TECHNICAL COMPARISON BETWEEN NPC AND CHB INVERTERS

Characteristic	5-Stage NPC Inverter	5-Stage CHB Inverter
Voltage Levels per Phase	Five levels (±2Vdc/2, ±Vdc/2, 0)	This inverter operates on five levels, which is achieved through the combination of two cascaded H-bridges.
Configuration	Single DC source equipped with clamping diodes	It utilises multiple isolated DC sources or battery stacks
Overall Harmonic Distortion	Approximately 4.5%–5.5% (when utilising appropriate SPWM)	The efficiency ranges from approximately 2.5% to 3.5%, which is improved due to the presence of more voltage vectors.
Complexity of Control	Medium (involves diode balancing alongside multilevel PWM)	The design is characterised by high performance, with individual PWM control for each H-bridge ensuring voltage balance.
Modular Design	Low (pertains to a single unit)	It is also noted for its high modular design.
Fault Tolerance	Poor (a malfunction in one device impacts the entire system)	The system is advantageous as one module can be bypassed if necessary.
Requirement of DC Supply	Commonly utilised DC bus	Additionally, it incorporates multiple isolated sources or transformers.
Effectiveness	Medium (higher switching loss from clamping)	The performance is enhanced, being optimised for each module.
Dimension & expenses	Compact design with a reduced component count	However, it is bulkier and more costly due to the requirement for multiple modules.
Integration with the grid	Standard (necessitates a neutral point)	Overall, it is excellent, particularly in applications involving renewable energy integration.

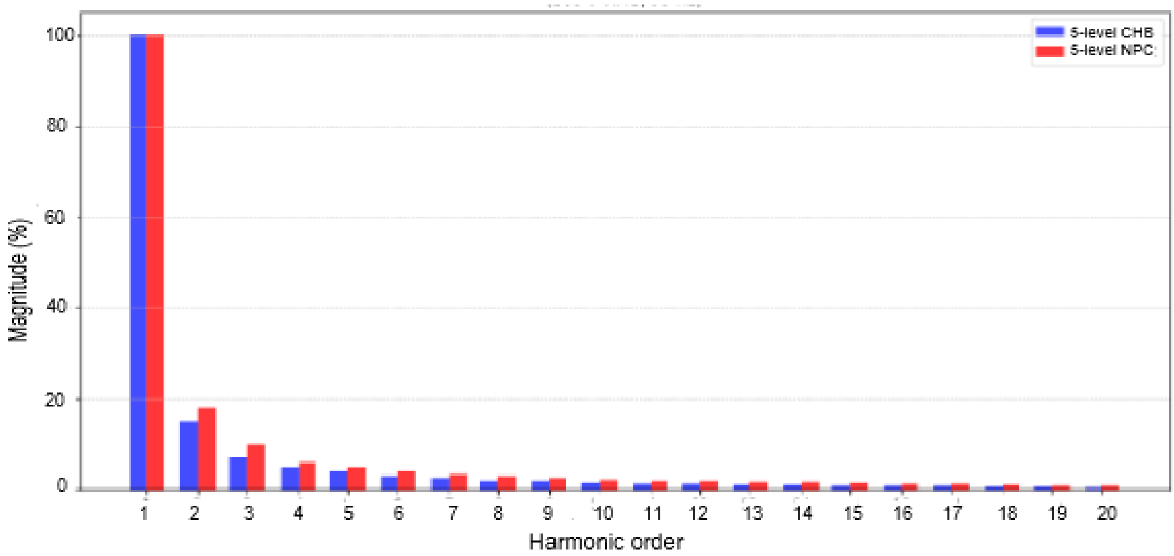

Fig. 5. Total Harmonics generated by the two topologies, CHB and NPC inverters, specifically the 5-level NPC and CHB inverters operating at 380 V RMS and 50 Hz.

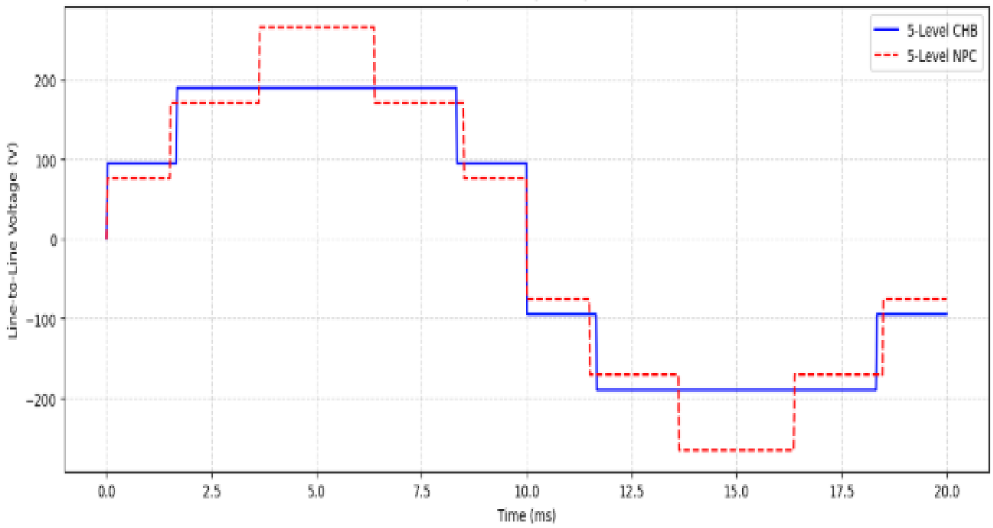

Fig. 6. Comparison of the output voltage waveforms comparison 5-level at 380 V (L-L), 50 Hz for (NPC vs. CHB)

D. Output voltage waveforms comparison (NPC vs. CHB)

Figure 6 shows the comparison of the output voltage waveforms of 5-level at 380 V (L-L), 50 Hz for (NPC vs. CHB). It shows the simulation comparison and the results, so we can see the difference in output waveforms and harmonics between a 5-level NPC and a 5-level Cascaded H-Bridge (CHB).

4- Conclusion

This study presents a comparative analysis of the THD performance of five-level, three-phase inverters implemented using CHB and NPC topologies. The investigation is carried out under identical operating conditions at 380 V RMS and 50 Hz, using MATLAB/Simulink for modelling and harmonic analysis. The findings offer significant assistance for choosing an acceptable MLI architecture for manufacturing, renewable energy, and high-power electronic applications by illuminating the compromises among harmonic performance, complexity of structure, and execution feasibility. Practical methods for lowering THD include filter design, suggested switching frequencies, modulation adjustments, and compromises between NPC and CHB. Final accomplishments: Although NPC's ease and considerably smaller element size, CHB outperforms NPC in THD and harmonic efficacy for five-level three-phase systems.

TABLE VI. THD COMPARISON SUMMARY (SIMULATED/EXPECTED VALUES)

METRIC	5-STAGE NPC	5-STAGE CHB
THD (%)	~4.8%	~2.9%
HARMONIC ORDER DOMINANCE	5TH, 7TH	11TH, 13TH (LOWER MAGNITUDE)

An overview of THD evaluations is presented within Table VI, and the Cascaded H-Bridge (CHB) arrangement exhibits both flexibility and Total Harmonic Distortion (THD). exceptional performance. On the other hand, the Neutral Point Clamped (NPC) arrangement turns out to be more beneficial when considering Convenience and Expense.

TABLE VII. THE OPTIMAL SELECTION IS THE BEST CHOICE

For the type of application	The optimal selection is the best choice	Provided Justification
Industrial electrical machine Drives	NPC	Reduced expenses, established configuration.
Solar Photovoltaic and Energy Storage Systems	CHB	Modular and high-quality waveforms from various sources
Compact Inverter apparatuses	NPC	A reduced footprint with centralized control

Table VII shows that the ideal choice is the most effective alternative for specific kinds of activity.

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